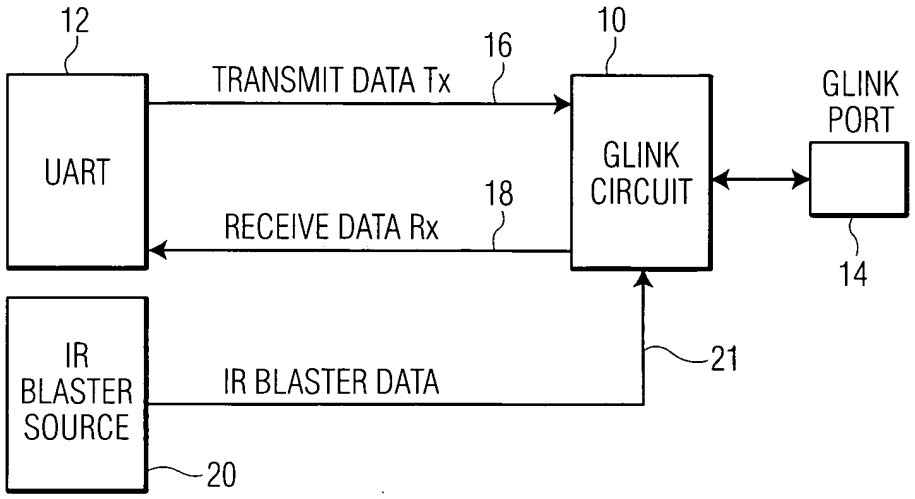

FIG. 1
PRIOR ART

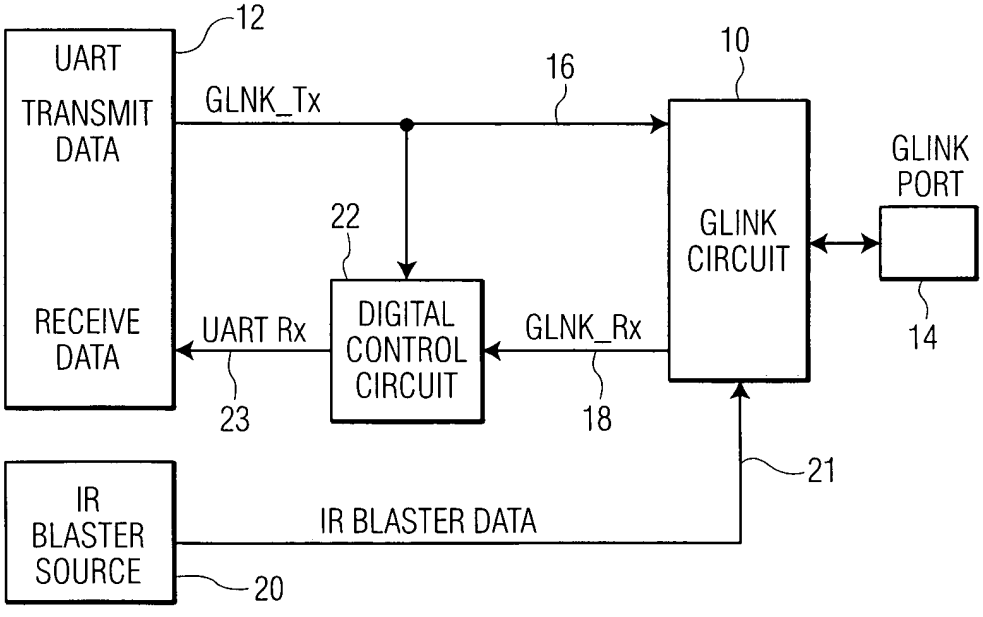

FIG. 2

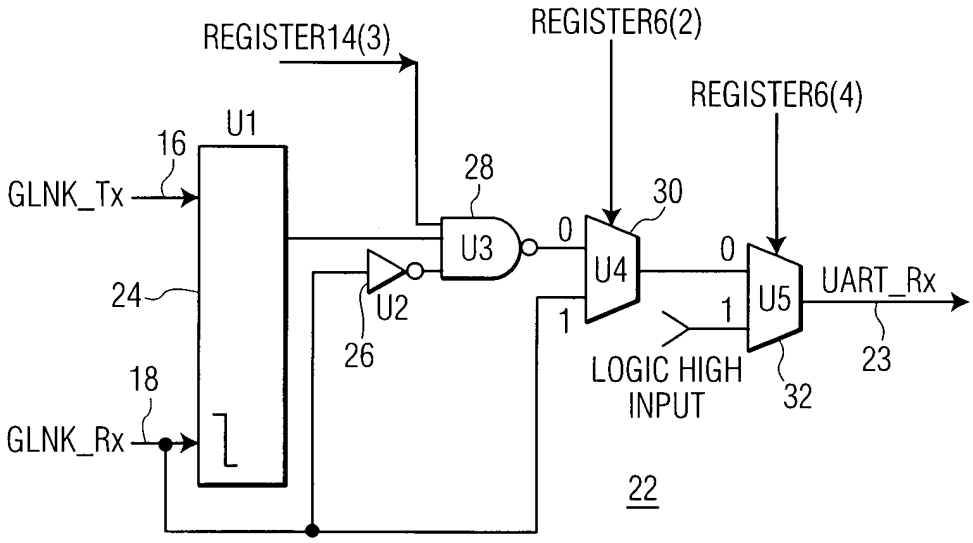

FIG. 3A

DIGITAL CONTROL CIRCUIT							
MODE	CPLD CONTROL REGISTERS			CPLD DATA INPUTS		UART INPUT	COMMENTS
SETUP #	REGISTER6(4)	REGISTER6(2)	REGISTER14(3)	GLNK_Tx	GLNK_Rx	UART_Rx	
1 (MODE 1)	0	0	1	1	X	= GLNK_Rx	DEFAULT SETTING
2 (MODE 1)	0	0	1	0	X	LOGIC 1	DEFAULT SETTING
3 (MODE 1)	0	0	0	X	X	LOGIC 1	IR BLASTER ACTIVE
4 (MODE 2)	0	1	0	X	X	= GLNK_Rx	CONFIGURATION TEST MODE
5 (MODE 3)	1	X	X	X	X	LOGIC 1	DETECTED DEMO PIN

X: DON'T CARE IF LEVEL IS LOGIC HIGH OR LOW

FIG. 3B

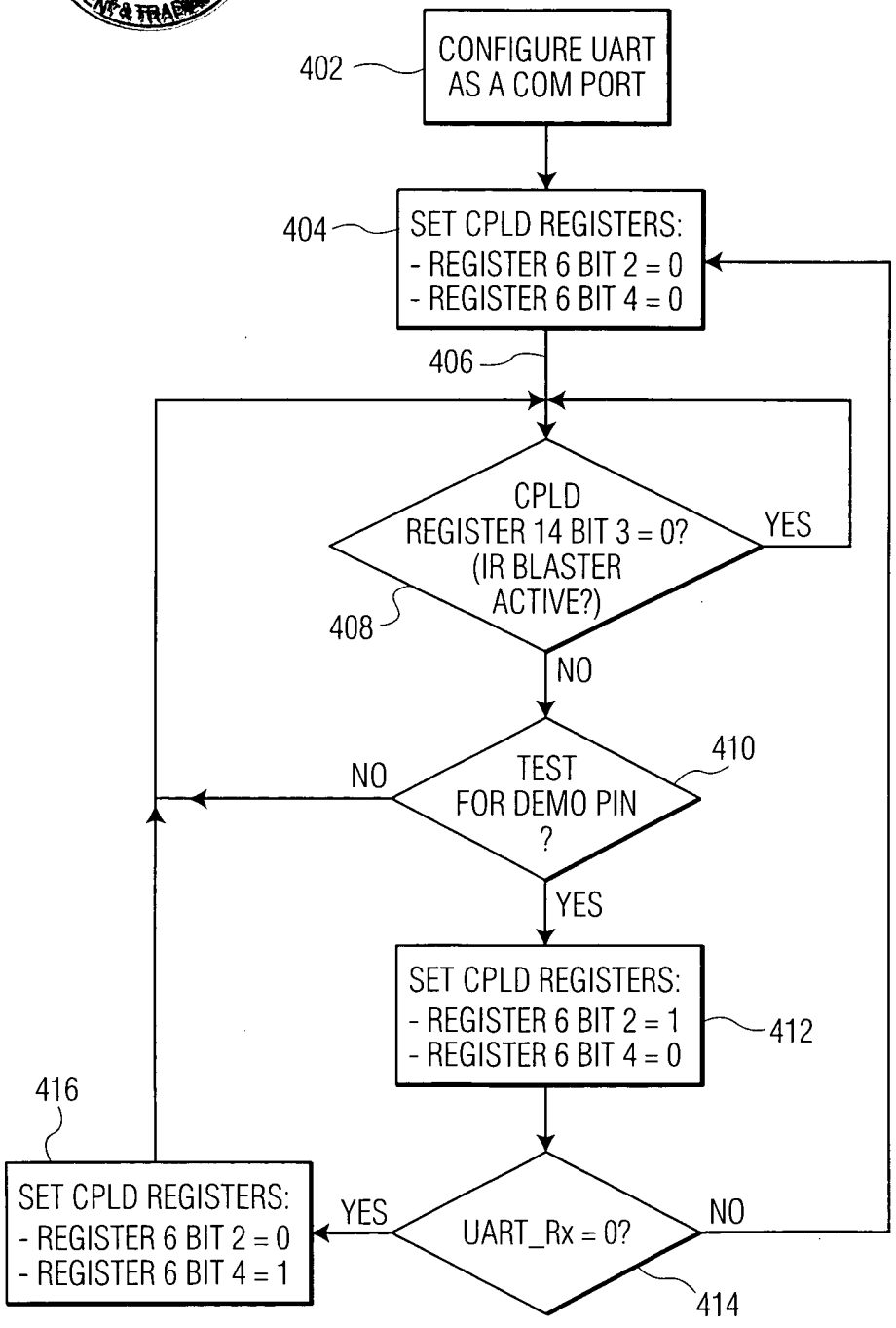

FIG. 4

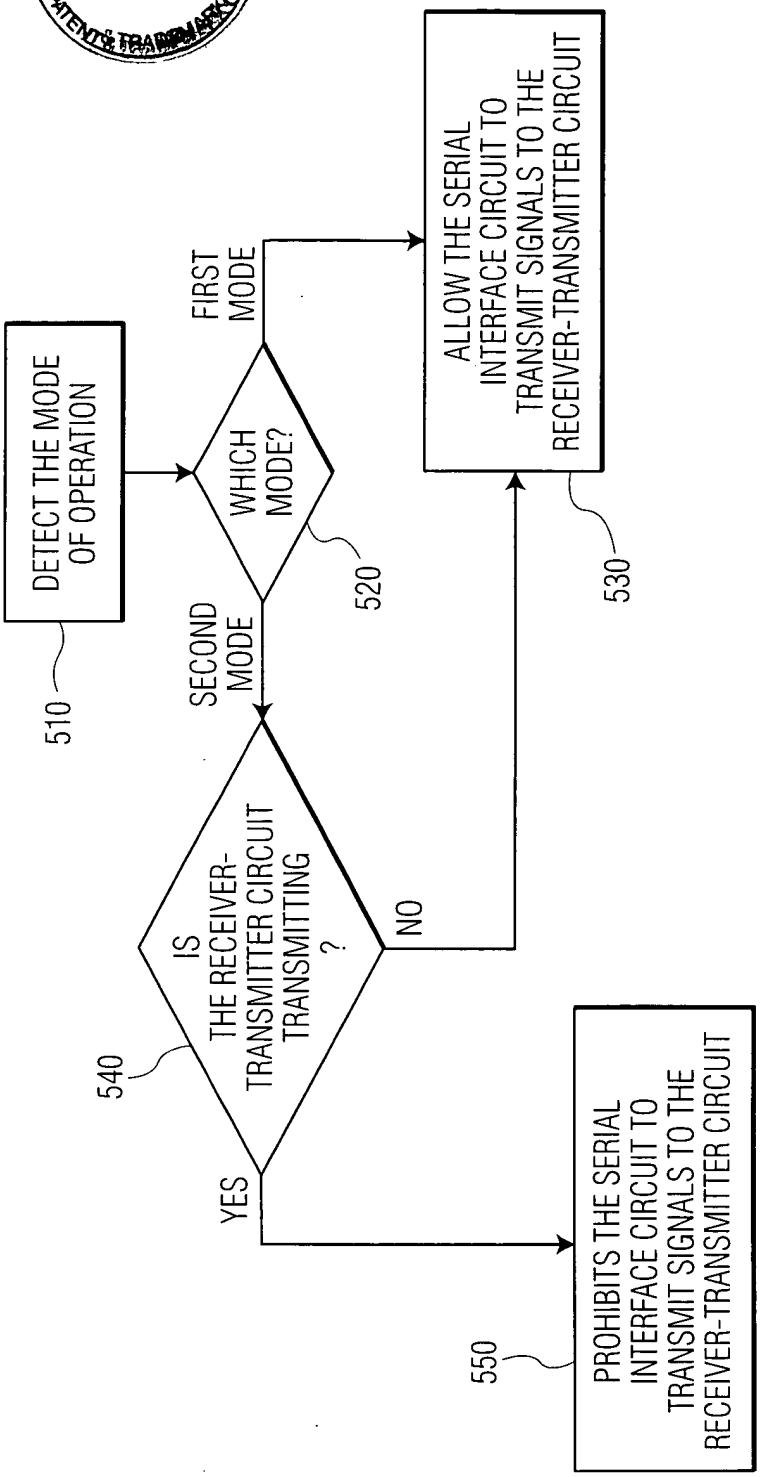

FIG. 5